Optimal Thermal Design for Chip Placement in Multichip Modules

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Summary

The paper is to pursue the maximum uniformity of temperature distribution across multiple-chip modules (MCMs) through thermal optimal placement design of chips. In the paper, two indirect optimization formulations are introduced to model the thermal optimization problems. By anyone of these two formulations, the associated objective function, the total chip junction temperature, is formulated by an approximate macro model using either the response surface method (RSM) or a force function. Subsequently, together with some predefined geometry constraints, the optimization problem is formed and furthermore, is either transformed into an unconstrained optimization problem using the exterior penalty function (EPF) method and then solved in primal space using both the BFGS method and the particle swarm optimization (PSO) methodology or directly explored using the currently proposed finite element-based (FE-based) Force-Directed (FD) algorithm. The effectiveness and applicability of these two indirect approaches are demonstrated through several design case studies.

Introduction

In this study, the optimal thermal placement of multiple chips in various MCMs in natural convection is investigated. The problem attempts to seek the system temperature distribution as uniform as possible through the finding of optimal chip locations. Two distinct, indirect approaches are proposed in this investigation to handle the class of optimization problems. The first indirect approach integrates the RSM (see, e.g., [1]) and an optimization algorithm. For readily creating the approximate macro models of the chip junction response associated with specified design variables, FE simulations are applied. Furthermore, the EPF method [2] that applies an additional penalty function reflecting the violation of the constraints is employed to augment the objective function, and then, to transform the original constrained optimization problem into an unconstrained optimization problem that can be easily solved in primal space using various robust unconstrained optimizers. Solution of the unconstrained optimization problem is fulfilled in the study through two different types of updating schemes: 1) a conventional nonlinear programming scheme- the BFGS method [2] and 2) a novel evolutionary computation (EC) algorithm –the PSO methodology [3].

The second indirect approach is termed as the thermal FD method. The FD method has been extensively applied in optimal routing design in VLSI and printed circuit board (PCB). The basic idea behind the FD algorithm can be analogous to the Hooke's law in applied mechanics. It employs a repulsive and attractive force between two objects, respectively, to keep those unconnected objects apart and to define the degree of connections between two connected objects. In literature, several modified FD algorithms (see, e.g., [4]) have been introduced to

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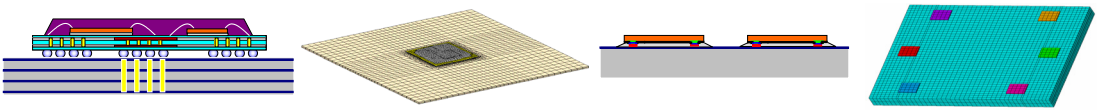
manage the thermal placement design of bare chips in a MCM. However, these FD algorithms are either not very robust and accurate or very complex in practical applications. Thus, an effective, improved thermal FD model, termed as the FE-based FD algorithm, is proposed in the study for thermal optimal design of MCMs. Essentially, the technique directly adopts actual temperature information that is obtained from FE analysis to build up the attractive and repulsive forces. Furthermore, geometry constraints are also taken into account in the model such that the overlapping problems between components could be also alleviated.

Problem Descriptions and FE Modeling

The study employs two classes of test vehicles for design as examples of validation of the proposed methodologies, including a planar, 256-pin, PBGA typed MCM that consists of three chips (Fig. 1-(a)) and several DCA typed MCMs containing a number of bare chips (Fig. 1-(b)). The MCM package is attached to a PCB of $114.3 \times 101.6 \times 1.57$ *mm*. On the other hand, the configuration of the DCA typed MCMs is simple in contrast to the PBGA typed MCM. The technology consists of three major components: an IC chip with gold micro-bumps, a circuit glass substrate with electrodes, and an anisotropic conductive adhesive (ACA) film. The size of the glass substrate is $50 \times 50 \times 5$ *mm* while that of these chips is identical, $5 \times 5 \times 0.5$ *mm*.

Full-scaled, 3-D thermal conductance FE models are used to perform numerical modeling of the thermal performance of these assemblies in natural convection. In the FE modeling, heat transfer mechanisms, including natural convection, radiation, and conduction are incorporated. The geometries of the assemblies are modeled in sufficient details; however, detailed thermal conductance modeling of certain components such as the PCB as well as BT substrate presents certain challenges due to their highly complicated geometries and structures. Consequently, the rule-of-mixture technique [5] is applied to explore the effective thermal conductance of the BT substrate and the PCB of the PBGA typed MCM and the adhesive layer of the DCA typed MCM. Furthermore, to characterize the assembly's surface heat transfer to the ambient through convection and radiation, existing empirical convective and radiative heat transfer coefficient correlation models [6,7] are utilized. It is particular to note that these convective and radiative heat transfer coefficients are applied at every surface point of the FE model to characterize the local surface heat transfer activity.

Two examples of 3-D meshes associated with the planar PBGA typed MCMs having three dice and the DCA typed MCM having 6 dice are also shown in Fig. 1-(a) and -(b), respectively. In summary, sizes of these models range from about 5,000 to 25,000 solid elements.



(a) The PBGA typed MCM (b) The DCA typed MCM

Fig. 1 A schematic plot of the test vehicles and their associated FE model

Optimization Formulation I

The first indirect optimization formulation is fulfilled by integrating the RSM and an optimization algorithm. Note that the spatial locations of these chips embedded in the electronic

assemblies are considered as the design variables, and the total chip junction temperature in the designed system is defined as the objective. The RSM is thus applied herein to construct the macro approximate models of the chip junction temperature, obtained from FE modeling, associated with the design variables. The RSM requires an iterative process to construct the macro response surface for the desired system response. First of all, the mathematical form that can express appropriately the relation of the chip junction temperature and the chip locations is assumed. In the work, a quadratic nonlinear regression model is adopted. Next, an appropriate experimental design plan, i.e., the Central Composite Design [8], is determined, in which it consists of limited and selected design points, for which the simulations are accordingly performed. In this study, numerical simulation that adopts FE analysis is applied for carrying out the chip junction temperature associated with selected design points. At last, by using regression analysis, the response surface is determined based on these response data gathered from the experiments. The validity of the macro model is extensively examined through two approaches: 1) the examination of the relative and absolute errors between the FE analyses and the estimated responses, and 2) statistical tests, including *F*-test and R^2 test (see, e.g., [9]).

With these approximate chip junction temperature expressions together with the geometry constraints defining the non-overlapping condition of the chips, the multi-objective optimization sub-problem can be accordingly formulated using a l_1-*norm* composite objective formulation. Furthermore, by using the EPF method, the constrained optimization problem is then transformed into an unconstrained problem:

$$\text{Minimize} \quad F(X,Y,r_g) = \sum_{l=1}^{n} T_j^l(X,Y) + P(X,Y,r_g) \tag{1}$$

Subject to

$$X^B \le X \le X^U, \quad Y^B \le Y \le Y^U \tag{2}$$

where Eq. (2) presents the side constraints of the design variables, in which the superscript "*B*" and "*U*" denote the upper bound and lower bound of the associated design variable, respectively, and $P(X,Y,r_g)$ represents the penalty function defined through the penalty constant r_g. It is expressed as:

$$P(X,Y,r_g) = r_g \left[\sum_i \left(Max\{0, g_i(X,Y)\} \right)^2 \right] \tag{3}$$

In the penalty function, $g_i(X,Y)$ represent the non-overlapping constraints on the chips. If any inequality constrain is not satisfied, a square penalty of the violation is added to the objective function. The transformed unconstrained problem solves the original constrained problem as r_g approaches infinity.

The unconstrained optimization problem is explored by using both the mathematical programming (MP) technique and the EC algorithm. Specifically, they are the BFGS method and the PSO algorithms, respectively. The BFGS method is a rank-two update scheme for the inverse Hessian approximation. Numerical evidences show that the BFGS method is a superior to all known variable-metric algorithms, and thus is applied in the study. On the other hand, akin to genetic algorithms (GAs) that are primarily based on the Darwinian rule of the selection of the fittest, the PSO algorithm is a natural process for exploring optima, in which it is motivated by the behavior of organisms such as fish schooling and bird flocking. It combines social psychology principles in socio-cognition human agents and EC, and implies the features of both GA and ES. The initial search is performed by a population of randomly-picked potential

solutions or particles. These particles fly around in *n*-dimensional hyperspace to search for the location of the optimal. The evolutionary process is terminated when the coordinates of there particles remain unchanged or when the limit of iteration is reached.

Optimization Formulation II

The optimization problem is alternatively tackled by using the proposed FE-based FD algorithm. Instead of adopting the predefined *Z* function as attractive forces and its complement member, the *S* membership function, as repulsive forces, which are used in fuzzy-logic-based (FL-based) algorithm [4], the current FD algorithm applies actual system temperature information, which is obtained from FE modeling, to characterize the thermal relation between any two chips. The attractive force herein represents the degree of the thermal interaction of a single chip itself with the system and environment. Thus, the junction temperature of the chip is considered as the attractive force. To facilitate the calculation of these attractive forces, the RSM is applied to create, through a limited selected design sampling points, the corresponding attractive-force response surface associated with the spatial location of the chip. On the other hand, the repulsive force denotes the thermal interaction of a chip with any other one. In other words, the temperature increment of a chip due to the thermal interaction with the other joining chip is defined as the repulsive force. Furthermore, the repulsive force of any two chips separated by any distance is also calculated by using FE modeling techniques. Likewise, for simplification, numerical calculation of the repulsive forces is fulfilled at some limited pre-selected sampling design points. Furthermore, with the modeled results, an interpolation scheme is applied to produce the corresponding repulsive-force macro curves associated with the separated distance of the chip.

The resultant force of the entire design system can then be determined by:

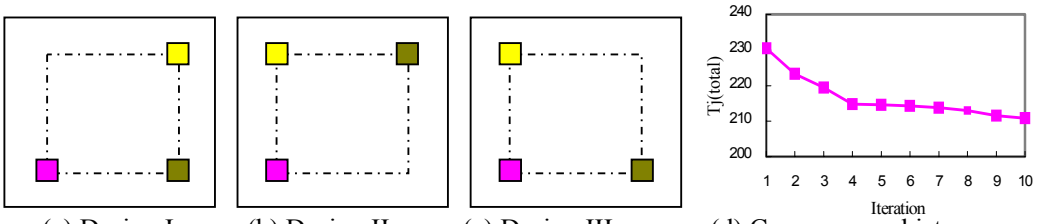
$$F = \sum_{i=1}^{n} A_i\left(X_i, Y_i, \Theta\right) + \sum_{i=1}^{n} \sum_{p=i+1}^{n} R_{ip}\left(d_{ip}, \Theta\right), \tag{4}$$

where $A_i\left(X_i, Y_i, \Theta\right)$ represents the attractive force of the *i*-th chip under the power density Θ and at the spatial location (X_i, Y_i), and $R_{ip}\left(d_{ip}, \Theta\right)$ denotes the repulsive force between the *i*-th chip and *p*-th chip with a separated distance d_{ip}. The problem can then be converted into seeking a design (i.e., optimal thermal placement) associated with a minimized total force exerted on the design system. In the approach, geometry constraints for preventing chips from overlapping are also implemented. Based on the resultant force in the design system as the objective together with those geometry constraints, the finding procedure for the optimal solution can be very straightforward and efficient. It should be noted that the procedure requires a random function to generate an initial random placement location of these chips. Once the resultant force attains a minimal value, convergence is achieved and the iteration procedure is terminated.

Design Applications

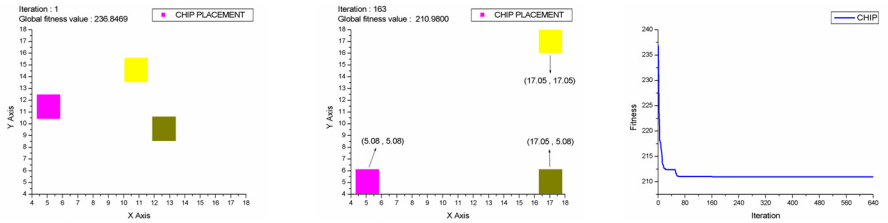
The thermal placement design of the PBGA typed MCM is first tackled by the optimization formulation I using the BFGS method. The permissible spatial range (the upper and lower limit of the design variables) for these chips in the MCM to change is limited to [5.08, 17.05]. In the

design, the heating power for each die is $1.0W$ and the ambient temperature is $25.0^{o}C$. Basically, the BFGS method is a local optimizer; hence, the obtained local solutions should be dependent of the initial guess of these design variables. By using three different initial guesses, we actually obtain three various final designs, shown in Fig. 2-(a), -(b) and -(c), respectively. Theoretically, based on the symmetric configuration of the MCM and the same power density applied for each die, these three final designs are all the global optimum, despite that they are merely local optima of the technique. Furthermore, the convergence history of the objective function for one of the above optimal solutions is also shown in Fig. 2-(d), in which it is monotonically and effectively converged toward the optimal.



(a) Design I (b) Design II (c) Design III (d) Convergence history

Fig. 2 Optimal placement designs of the PBGA typed MCM using the BFGS method



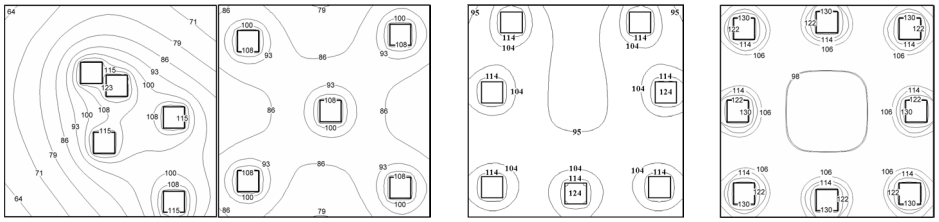
(a) Initial design of chips (b) Final design of chips (c) Convergence history

Fig. 3 Optimal placement designs of the PBGA typed MCM using the PSO algorithm

These optimal results are further validated by the PSO methodology. The total number of particles considered in the design is 30 and each particle is composed of 6 degree of freedom representing the spatial coordinates of these chips. Fig. 3-(a) presents the initial random location of these three chips. One of the final optimal designs of the planar BGA typed MCMs is shown in Fig. 3-(b). The optimal result is exactly identical to that of the BFGS approach. In contrast to the BFGS method, it would be more difficult for the approach to explore the other two solutions, as shown in Fig. 2-(b) and -(c). This is due to that there is a certain degree of inaccuracy in the approximate macro models despite that it is proved minimal; as a result, some differences are implied in the "estimated" objective function associated with these three optimal designs. Since the PSO is a global optimizer and more importantly, the current optimal design indeed provides the minimum "estimated" objective function, the current optimal design is accordingly derived. At last, the history of convergence of the objective function is presented in Fig. 3-(c). Evidently, a slow convergence rate is obtained by the approach, as compared to the BFGS method.

Thermal optimal placement design of three examples of DCA typed MCMs, respectively containing 5, 7 and 8 chips, are illustrated using the proposed, modified FE-based FD algorithm. The dissipation power of these chips is exactly the same, and equal to 1 *Watt*. The initial design of the 5-chip design practice and its corresponding temperature contour obtained from FE analysis are shown in Fig. 4-(a). By these force functions as well as the aforementioned constraints, the final thermal optimal placement designs associated with these design examples

are illustrated in Fig. 4-(a), -(b) and -(c), together with the corresponding modeled temperature distributions. It can be first detected in Fig. 4-(a) that the optimal design reduces the chip junction temperature significantly and also, presents a much more uniform temperature distribution across the assembly in contrast to its corresponding original design. By further compared the total force in each chip of the 5-chip system with the associated FE analysis results, the difference in terms of the chip junction temperature ranges only 0.6~1.3%. This demonstrates the capability and accuracy of the proposed force functions in characterizing the temperature field of these chips.



(a) Initial and final designs of 5-chip case (b) 7-chip design (c) 8-chip design

Fig. 4 Optimal placement designs of the DCA typed MCM using the proposed FD algorithm

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